

Docket No. 240800US2S DIV

IN RE APPLICATION OF: Norihisa ARAI

SERIAL NO: 10/670,529

FILED: September 26, 2003

FOR: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE INCLUDING PROCESS FOR IMPLANTING IMPURITIES INTO SUBSTRATE VIA MOS TRANSISTOR GATE ELECTRODE AND GATE INSULATION FILM



*JPW*

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

Transmitted herewith is an amendment in the above-identified application.

☒ No additional fee is required

☐ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.

☐ Additional documents filed herewith:

The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	15	MINUS	20	0	x \$50 =	\$0.00
INDEPENDENT	3	MINUS	3	0	x \$200 =	\$0.00
		<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS			+ \$360 =	\$0.00
		TOTAL OF ABOVE CALCULATIONS				\$0.00
		<input type="checkbox"/> Reduction by 50% for filing by Small Entity				\$0.00
		<input type="checkbox"/> Recordation of Assignment			+ \$40 =	\$0.00
		TOTAL				\$0.00

☐ A check in the amount of \$0.00 is attached.

☐ Credit card payment form is attached to cover the fees in the amount of \$0.00

☒ Please charge any additional Fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

☒ If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

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DOCKET NO: 240800US2S DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF

:

NORIHISA ARAI

: EXAMINER: ROSE, KIESHA L.

SERIAL NO: 10/670,529

:

FILED: SEPTEMBER 26, 2003

: GROUP ART UNIT: 2822

FOR: METHOD OF MANUFACTURING  
SEMICONDUCTOR DEVICE INCLUDING  
PROCESS FOR IMPLANTING  
IMPURITIES INTO SUBSTRATE VIA  
MOS TRANSISTOR GATE ELECTRODE  
AND GATE INSULATION FILM

AMENDMENT

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

In response to the Office Action dated October 5, 2004, please amend the above-identified application as follows:

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper.

**Remarks/Arguments** begin on page 7 of this paper.